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(12) **EUROPEAN PATENT APPLICATION**

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(54) Coded information arrangement.

(57) An active transponder device comprises a CMOS inte-
grated circuit including means (21) for receiving an input
signal including coded information, a memory (31) for storing
said information, and transmitter means (24) for transmitting
an output signal including said information, the input signal
and the output signal being both low frequency induction
communication signals.

Normally, the output signal is emitted in response to an
interrogation signal received via the receiving means (21),
and is formed by modulation of that signal with said informa-
tion after readout from the memory. The transponder oper-
ates inherently synchronously, using a single master clock
signal which is generated either in an interrogation transmit-
ter or in the programmer for injecting the coded information.

The integrated circuit has a second receiving means (41)
used in the injection of the coded information. The injection of
a clock-pulse which is in synchronism with the input signal
enables the memory (31) to receive the coded information.

The transponder may be used for the identification of e.g.
people or articles at the limits of a particular area e.g. a store.

EP 0 040 544 A2

- 1 -

CODED INFORMATION ARRANGEMENT

The present invention relates to an arrangment for detecting coded information and more particularly to an arrangement in which the code is held on an active transponder. Such arrangements are useful in the identification of articles, or to control the entry of personnel to zones of limited access, for example.

One such arrangement is shown in Figure 6 of Patent Application GB 2017454A. A circuit is provided with an encoder in the form of a data coding chip. The chip comprises a plurality of diodes, selected ones of which are blown to permit a unique serially coded pulse train to be produced. A disadvantage of this previous arrangement is that once the code has been selected it cannot be readily changed. However, the use of a chip containing all relevant circuitry is a very economical way of manufacturing a transponder in large numbers. It would be a considerable advantage if such a transponder could be produced in which the coding could be changed at will.

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British Patent Specification No. 1 555 606, supported by its Parent Patent No. 1 538 157, describes a transponder in which a unique code is stored in a memory and can be changed. However, this system is on a very different scale since the transponder is to be mounted on vehicles, its weight is not critical, and its manufacture would be extremely expensive. It operates exclusively using high frequency electromagnetic signals (10 GHz) and waveguides. Such a device requires relatively high current levels for its operation, and therefore requires a larger battery or more frequent changes.

The invention aims to provide a cheap. lightweight mass-produced transponder of low current consumption.

According to one aspect of the invention, there is proposed an active transponder device comprising a semiconductor integrated circuit including means for receiving an input signal including coded information, a memory for storing said information, and transmitter means for transmitting an output signal including said information, the input signal and the output signal being both low frequency induction communication signals.

The use of the low-frequency induction communication band (up to 150 KHz) enables the use of CMOS chips which have very low quiescent current consumption.

Normally, the output signal is emitted in response to an interrogation signal received via the receiving means, and is formed by modulation of that signal with said information after

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readout from the memory. The transponder operates inherently
synchronously, using a single master clock which is generated
either in an interrogation transmitter or in the programmer for
injecting the coded information. This ensures very high integrity
operation and requires only minimal verification to ensure valid
signals.

Preferably, the integrated circuit has a second receiving.
means used in the injection of the coded information. The use
of this second receiving means for injection of a clockpulse which
is in synchronism with the input signal enables a very high level
of program protection to be achieved before the memory is enabled
to receive the coded information. Moreover, the dual signal input
allows the use of a simple, cheap integrated circuit.

In accordance with a second aspect of the invention, there
is provided a detector system comprising means for emitting a
low-frequency induction communication signal, an active transponde
device, responsive to such input signal, having a memory for stori
coded information and transmitter means for producing an output
signal formed by modulation of the input signal with the coded
information, and means for receiving the transponder output signal

A preferred embodiment of the present invention will now be
described by way of example only, with reference to the accompanyi
drawings, of which:

Figure 1 shows a block diagram of a programmable coded
tag constituting an active transponder, and

Figure 2 shows a block diagram of an interrogator associated
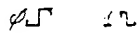with the coded tag of Figure 1.

Referring to Fig. 1 there is shown in block diagram from

the circuitry of an active transponder 10 which is mounted on a

programmable tag 20. The circuitry is a semiconductor integrated

circuit of CMOS type, designed for operation in the inducted

frequency communication bond i.e. up to 150KHz. The transponder

emits a phase coherent response at a sub-harmonic of an interro-

gating transmission; such a transponder is disclosed in Patent

Application GB 2017454 A.

A receiver 21 comprises a self-biasing input stage, used as

an RF amplifier for the interrogation signal which is transmitted

at a frequency of 132 KHz and two inverters, 25, 26. The detected

interrogation signal is fed via a further inverter 27 to a

frequency translator 22 which divides the signal by a factor of two

to provide a 66 KHz re-transmission carrier.

The output of receiver 21 is also supplied to a detector circuit

29, and the output of inverter 27 is also supplied to a counter reset

circuit 28. The 66 KHz carrier signal from frequency translator

22 is fed to a modulator 23 comprising an AND gate   where the car-

rier is modulated by the code data word. The 66 KHz carrier

signal is also supplied to a divide-by-384 counter 34.

The modulated signal is then supplied to a transmitter 24

which comprises a buffer amplifier supplying a re-transmit aerial

with a power boosted signal.

The encoding circuitry of the programmable tag comprises

a code data memory register 31 which stores the programmed code data

A memory addressing circuit comprises an N-Bit data selector 32,
the memory data digit output of which is determined by an indexing
counter 33. Counter 33 receives clock pulses from the counter 34.
An output data formatting circuit is constituted by a half-bit
forming circuit 36 which is an exlucsive - OR gate; a selected data
digit is combined with the output of the clock counter 34 to form
a half-bit data transmission format. Thus data 'zero' is transmitted
at '0' for half the time followed by '1' for the remaining half,
with complementary transmissions for data 'one'.

For use in programming the tag 20, a second R.F. receiver
41 is provided. The output of receiver 41 is fed via an AND gate
42 to the clock input of code memory register 31. AND gate 42 is
part of an inhibiting circuit 43 serving to protect the memory by
preventing accidental clocking of the code memory register. The
inhibiting circuit 43 also comprises a divide-by-4 counter 44, a
D-type flip-flop and a pulse counter 46.

Referring now to Fig. 2, there is shown an interrogator for
use with the coded tag 20. A master 132 KHz oscillator 50 feeds both
the transmitter 51 and a system central timing unit 52. A 66 KHz
signal emitted by the active transponder 10 on tag 20 is detected
by a receiver 53. The output of a receiver tone decoder 54 is fed
into a (2N + 2) stage shift register 56 under the control of the
central timing unit 52. A half-bit format detector 57 checks the
half-bit format and an N-Bit latch 58 acts as a temporary store for
the data. The data is subsequently transferred to a second N-bit

004054

latch 60 whose contents are compared with latch 58 by a comparator
59. A noise gate 62 is also provided to permit unwanted noisy
signals to be rejected. A 'zero' detector 63 is connected to shi
register 56.

The normal mode of operation of the arrangement will now be
described. Assuming initially that the tag 20 is remote from a
sensitive zone and that is there is no 132 KHz singal present at
its input, then the output of inverter 25 is high (a logic '1') an
the output of inverter 26 is low (a logic '0'). Thus the code dat
input supplied by detector circuit 29 to the code memory register
31 is also low. The output of inverter 27 is high, causing a
reset signal to be applied to all of the counters and other
sequential logic functions establising a known initial state.

When the tag is intorduced into a sensitive zone, it receive
a 132 KHz continuous signal and the reset signal is removed, thus
enabling all the counters. Frequency translator or divider 22
then supplies a 66 KHz carrier supply signal to the modulator 23 an
counter 34 to provide a clock pulse for indexing counter 33 and
the half-bit forming circuit 36. The indexing counter is thus
advanced from zero at a pulse repetition interval of 5.82 milli-
seconds. A data output of zero is required initially such that th
data input to the modulator 23 is low for 2.91 milliseconds and
high for the next 2.91 milliseconds in half-bit format. This
technique prevents the coded tag responding to a transmission
from a presence sensing tag system which transmits 132KHz for
2.0 milliseconds at 35 millisecond intervals. Such a system is

disclosed in the above-mentioned patent application GB 2017454A.

The indexing counter 33 is advanced one count at the end of the

initial 5.82 milliseconds causing the first code data digit store

in the memory register 31 to be output in half-bit format. This

sequence repeats until all code data digits been addressed and

output in half-bit format, after which time the 132 KHz interrog-

ation transmitter 51 is switched off for a period of some 20 to 5

milliseconds in order to permit auto-resetting to occur in readin

for the next interrogation. In this way a coded tag transmits a

66 KHz signal amplitude modulated by its unique code and incorpo-

rating a leading zero. The total time between interrogation cycl

is therefore $N \times 5.8 + 35 \pm 15$ milliseconds, e.g. 175 ± 15 milli-

seconds for a 24 - Bit code.

A leading one or zero may be permanently programmed during

manufacture of the tag by strapping of the first memory location

(0 in Fig. 1). This will allow the tag to respond if required to

the presence sensing system mentioned above.

During each interrogation cycle the central timing unit 52

gates the 132 KHz carrier 'on' for a period equal to $(N + 1) \times 5$.

milliseconds, where N is the number of code Bits. A serial digit

Bit stream corresponding to the coded response signal transmitte

by the active transponder 10 of the tag is fed into the $(2N + 2)$

stage shift register 56 under the control of timing unit 52. Up

completion of the $(2N + 2)$ clock pulse cycle, the code format is

checked for the correct half-bit format and if valid the data is

dumped into a temporary store consisting of the first N Bit Latc

The decoding process is enabled upon satisfactory detection of the leading zero by detector 63.

The data received from the next interrogation response is pushed into the first latch 58 once the original data has been transferred to the second latch 60. The results of two successive interrogation are compared at 59 and if a match is obtained the data is deemed valid and is then produced as an output for display alarm or further processing.

As many comparisons as required may be carried out. For example further comparators and latches may be provided, or a plurality of "data valid" signals may be counted before the central timing unit is actuated to produce an output.

Whilst the received signal is being fed to shift register 56, it is also tested for noise transistions around the clocking instant by noise gate 62. If a '1' to '0' transition is detected during what should be a '1' signal, it is assumed that this is due to undesired noise and the data already received is destroyed by re-setting shift register 56. Thus instead of performing a whole transmission cycle, the cycle is terminated and a new cycle is commenced; this leads to a saving of time.

The programming mode of operation of the arrangment will now be described in which a desired code is applied to the tag 20. In this mode, the code data is transmitted to the 132 KHz receiver 21 and an inductively coupled r.f. code memory clock signal is applied to receiver 41. This avoids the need to radiate r.f. transmissions which in some countries requires a licence.

Also the high input signal level required to internally generate

a clock pulse gives added noise immunity to the system. The

receiver outputs are detected and fed respectively to the data and

clock inputs of the coded memory register 31. Once the inhibiting

circuit 43 is enabled to pass the clock signals, the memory is

programmed by the coded data stream signal. A normal interrogation

cycle is then carried out to validate the code.

The clock input of register 31 is inhibited for a period

corresponding to at least two interrogation transmission times

by the counter 44. The AND gate 42 is inhibited until the output

of the D-type Flip Flop 45 goes high which can only occur when the

correct whole number of pulses has been received at the programme

clock receiver 41 as determined by the pulse counter 46 and while

simultaneously a number of 132 KHz pulse corresponding to twice

the total count of the indexing counter 33 has been received. The

code programming cycle is thus longer than the normal interrogation

cycle.

An advantage of the above arrangement is that a user can

easily reprogram the coded data. This is of particular advantage

where such data is required for a short time only or where the data

contains some element which needs to be updated periodically. Exam-

ples of such uses are automatic baggage handling, mail bag routing

container identification. The data may relate inter alia to size,

weight, destination, date, time, price or other classification, as

well as including unique identification. A further advantage is that

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Also the high input signal level required to internally generate

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the reprogramming may be effected without making any physical

electrical contact with or disturbing the tag in any way. In

addition the tag only needs to be taken out of service for a very

short time at the user's convenience.

There is no limit to the number of reporgramming cycles which

may be undertaken during the service life of the transponder.

The number of possible codes is also very large indeed, the

only limit being imposed by the size of the chip used. Billions

of unique coxed may be utilised.

Due to the small physical size requirement of both the

transponder and interrogator, the roles are interchangeable i.e.

the interrogator may be static and used to detect the presence of

a transponder in the sensitive zone or alternatively, the

transponders may be fixed to large objects and a portable

interrogator used to "read" the codes for contents identification,

etc.

Various further modifications may be made to the above

arrangement, For example the active transponder could be mounted

directly on or could be an integral part of any article which it

is desired to detect.

In an alternative modification, the transponder may be

replaced by a 'free-running' device, which operates continuously

without the need for an interrogation signal. The signal

transmitted by the device contains coded information which may be

changed from time to time as desired.

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The device may be designed to operate anywhere in the induction communication frequency band.

4

CLAIMS

1. An active transponder device comprising means
for receiving an input signal including coded information,
a memory for storing said information, and transmitter
means for transmitting an output signal including said
information, wherein the receiving means (21), the
transmitting means (24) and the memory (31) are formed
as a semiconductor integrated circuit, and the input
signal and the output signal are both low-frequency
induction communications signals.

2. A transponder device as claimed in claim 1 wherein
said transmitter means (24) is fed from a modulator (23)
which forms said output signal by modulation of an
interrogation signal, received via the receiving means (21),
with said information.

3. A transponder device as claimed in claim 1 or 2,
comprising a program protection circuit (43) and a second
receiving means (41), the protection circuit being designed
to respond to a time relationship between the first signal
and a signal from the second receiving means to enable
the memory for storage of said coded signal.

2

4.   A transponder device as claimed in claim 3
wherein the signal from the second receiving means (41)
is a radio-frequency signal, at a pulse repetition
rate related to that of the first signal, and said time
relationship requires an exact whole number count
accumulation in a counter (46) within a period
determined by the first signal.

5.   A transponder device as claimed in claim 3 or 4
wherein the second receiving means (41) is adapted to
receive said radio-frequency signal by inductive
coupling of a closely adjacent emitter of a programming
device.

6.   A transponder device as claimed in any preceding
claim wherein said receiving means has a self-biassing
input stage.

7.   A transponder device as claimed in any preceding
claim wherein said memory (31), is addressed sequentially
by means of a digital counter signal produced by division
of a carrier signal frequency derived from the receiving
means.

8.   A transponder device as claimed in claim 7 wherein
in the absence of said carrier signal, a reset pulse
is applied to all counters and sequential logic members
of the device.

9.   A transponder device as claimed in claim 2, or
any claim appendant thereto, wherein the modulator
comprises an exclusive-OR gate (36) fed with data
at one input and a carrier pulse at the other, the
pulse rate being twice the data rate so as to produce
a half-bit data transmission format.

10.   A transponder device as claimed in any preceding
claim wherein a specified memory storage location
(31-0) is reserved and does not receive said coded
information, whereby its state is otherwise determined
and provides, as desired, a 'one' or a 'zero' in said
specified location independent of said information.

11.   A transponder device as claimed in any preceding
claim including a discriminator circuit (28) which
detected any asynchronous signal changes representing
noise, causes immediate termination of the function
then in progress, and initiates re-start of that function.

12.   A detector system comprising means for emitting
a low-frequency induction communication signal, an
active transponder device, responsive to such input
signal, having a memory for storing coded information
and transmitter means for producing an output signal
formed by modulation of the input signal with the
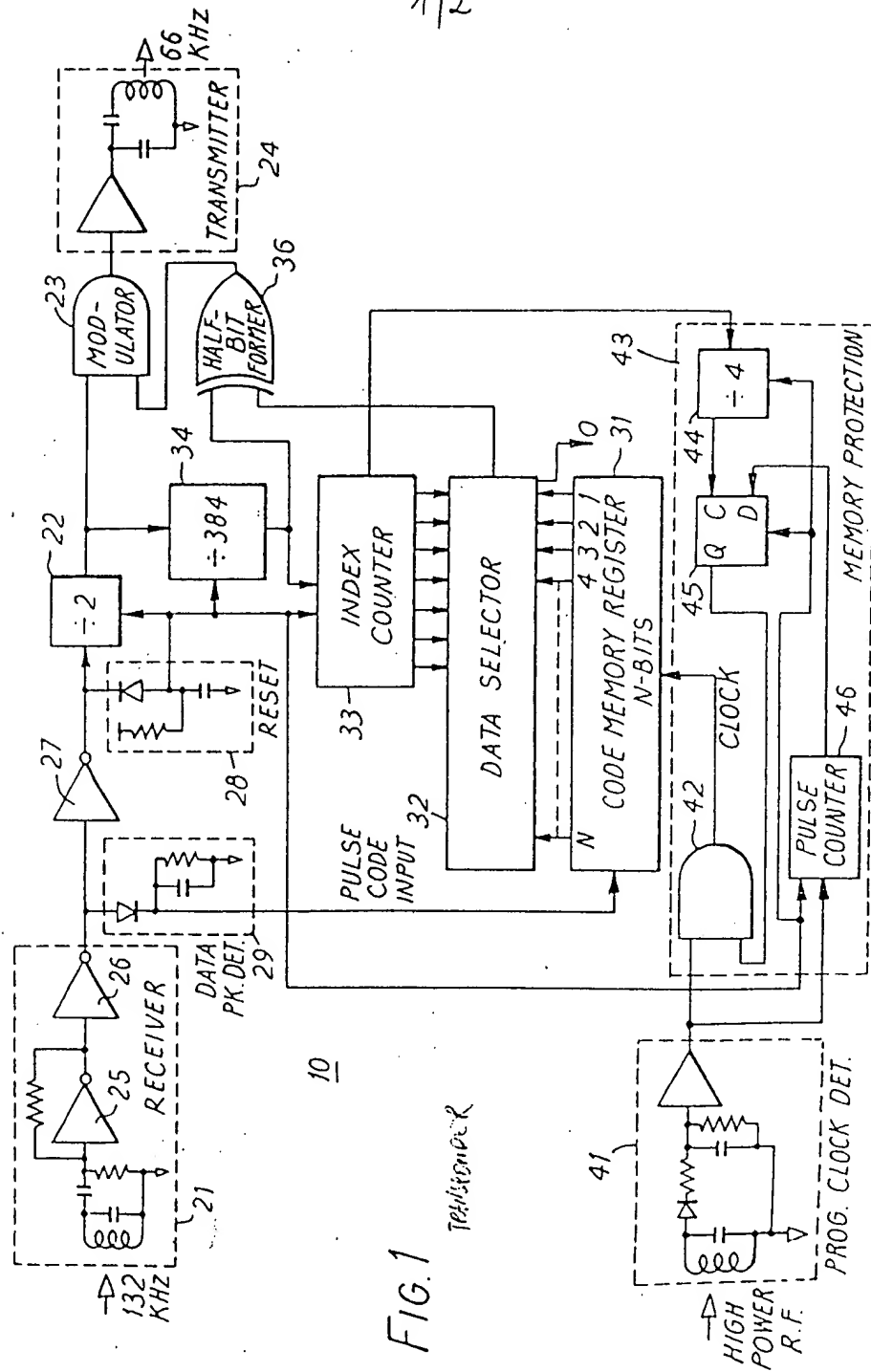coded information, and means for receiving the transponder
output signal.

FIG.1 TRANSCEIVER

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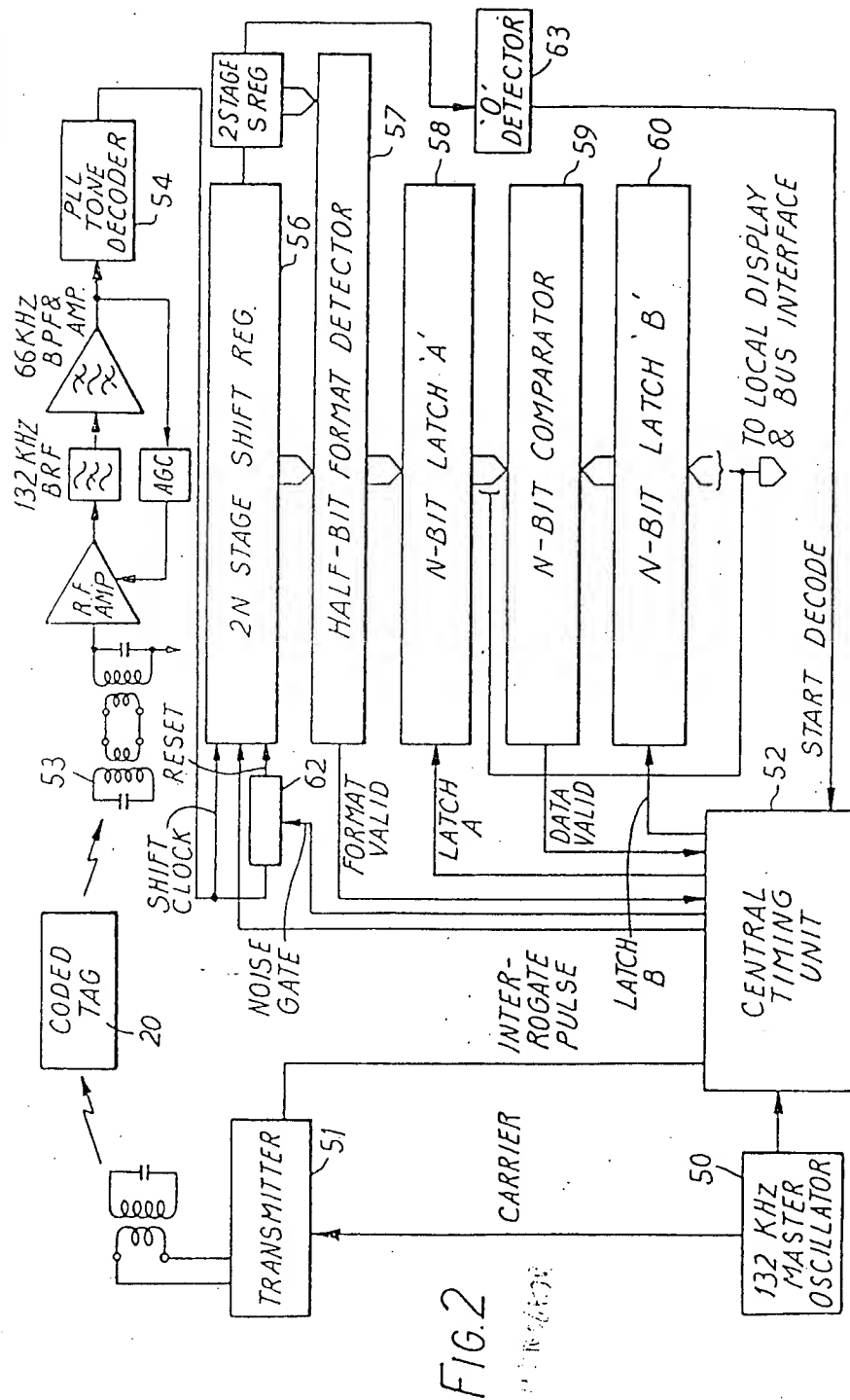FIG.2

European Patent Office

EUROPEAN SEARCH REPORT

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Application number

EP 81 30 2219

	DOCUMENTS CONSIDERED TO BE RELEVANT		CLASSIFICATION OF THE APPLICATION (Int. Cl.³)
Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	
X	GB - A - 1 555 606 (STIFTELSEN INST. FÖR MIKROVÅGSTEKNIK) * page 1, line 11 - page 2, line 108 * --	1-3,5, 12	G 01 S 13/78 G 08 G 1/12 B 07 C 3/12
	DE - A - 2 747 380 (ELECTROMATIC) * claims 1-10,13-15; page 8, lines 5-21; page 9, line 20 - page 10, line 31 * --	1,2,12	
	US - A - 3 766 523 (BROCKER et al.) * column 2, line 47 - column 9, line 19; figures 1-4 * --	1,2,12	**TECHNICAL FIELDS SEARCHED (Int. Cl.³)** G 01 S 13/78 H 04 B 5/00 G 06 K 19/06 7/08 B 07 C 3/12 G 08 B 3/10 G 08 G 1/12 B 61 L 25/04
	US - A - 3 859 624 (KRIOFSKY et al.) * column 10, lines 30-66; figure 8 * --	1,2,12	
A	GB - A - 1 427 920 (THE PLESSEY CO.) * claims *	1,12	

X The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
The Hague	14-08-1981	REEKMANS

CATEGORY OF CITED DOCUMENTS

X: particularly relevant
A: technological background
O: non-written disclosure
P: intermediate document
T: theory or principle underlying the invention
E: conflicting application
D: document cited in the application
L: citation for other reasons

&: member of the same patent family, corresponding document

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